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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,120	09/29/2000	Keith Glidewell	40921/205584	2023

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EXAMINER	
SHAH, NILESH R	

ART UNIT	PAPER NUMBER
2127	5

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,120	GLIDEWELL, KEITH	
	Examiner	Art Unit	
	Nilesh R Shah	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *29 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-20 are presented for examination.

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. Figure 1 is same as Fig. 1 of Patent 5,745,778.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alfieri (5,745,778) in view of Kimmel et al (6,105,053) (hereinafter Kimmel)

5. Alfieri was cited by applicant in IDS filed on 10/21/01

6. As per claim 1 Alfieri teaches the invention substantially as claimed including a method of allocating resources in a plurality of processors system each processor of said plurality having a cache associated therewith (fig. 1 element 100-108, col. 1 lines 33-36, col. 2 line 43), comprising:

when at least one processor of said plurality of processors system is idle, determining when at least one other processor of said plurality of processors is not idle (col. 8, lines 62-67)

and poaching a process on a queue of the at least one non-idle processor to be run by said at least one processor which is idle (col. 7 line 61 – col. 8 line 7, col. 9 lines 1-2)

7. Alfieri does not specifically teach the use of a predetermined period of time during which as least one processor remains not idle.

8. Kimmel teaches a method timing a predetermined period of time during which said at least one other processor which is not idle remains not idle and poaching a process when the predetermined period of time has elapsed (col. 14 lines 37-45) It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Alfieri and Kimmel because Kimmel's timing would maximize the throughput of the Alfieri's system by poaching a task from a non-idle processor to an idle processor only when the predetermined period of time has elapsed.

9. As per claim 2, Kimmel teaches a method wherein if more than one processor is idle, poaching the process with the idle processor which is electrically closest to the at least one non-idle processor (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45)

10. As per claim 3, Kimmel teaches a method wherein the time period during which a non-idle processor is allowed to remain non-idle is greater the farther away a non-idle processor is electrically located relative to an idle processor. (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45)

11. As per claim 4, Kimmel teaches a method wherein an idle processor will first try to poach from a non-idle processor electrically closest to it, and if the processor electrically closest to the idle processor is idle, it will then try to poach from the next processor which is electrically closest to it until it encounters a non-idle processor on which poaching can occur. (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45)

12. As per claim 5 Kimmel teaches a ccNUMA system (col. 4 lines 17-30)

13. As per claim 6, Kimmel teaches a method wherein each processor starts a timer associated therewith when it goes non-idle, and allowing an idle processor to poach a process therefrom only when a predetermined amount of time has elapsed

on the timer (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45).

14. As per claim 7, Kimmel teaches a method wherein said predetermined amount of time is established in relation to electrical proximity between an idle processor and a non-idle processor. (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45).

15. As per claim 8, Kimmel teaches a method wherein the greater the electrical distance between idle and non-idle processors, the greater the predetermined amount of time which is allowed to elapse for said non-idle processor (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45).

16. As per claim 9, is rejected for the same reason as claim 2 above. Alfieri did not specifically teach a method wherein said processor system is a four block system. However, Alfieri disclosed a multiprocessor system (Fig. 1) that could include a plurality of processors. It would have been obvious to one skilled in the art to have included 16 processors in Alfieri's system.

17. As per claim 10, Kimmel teaches a method wherein in the event more than one idle processors attempt to poach a process from a non-idle processor, allowing the idle processor in closest electrical proximity to the non-idle processor poach the

process (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45).

18. As per claims 11 –20, they are rejected for the same reason as claims 1-10 above.

19. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimmel et al (6,105,053) (hereinafter Kimmel)

20. As per claim 1 Kimmel teaches the invention substantially as claimed including a method of allocating resources in a plurality of processors system when at least one processor of said plurality of processors system is idle, determining when at least one other processor of said plurality of processors is not idle (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45)

and poaching a process on a queue of the at least one non-idle processor to be run by said at least one processor which is idle (col. 11 lines 4-7, col. 14 lines 37-45)

timing a predetermined period of time during which said at least one other processor which is not idle remains not idle and poaching a process when the predetermined period of time has elapsed (col. 14 lines 37-45).

21. Kimmel does not specifically teach each processor having a cache associated therewith. It would have been obvious to one skilled in the art to have included a cache for

each processor in Kimmel's system. By having a cache at each processor the access to memory will increase therefor increasing the throughput of the entire system.

22. As per claim 11 Kimmel teaches the invention substantially as claimed including a method of allocating resources in a plurality of processors system when at least one processor of said plurality of processors system is idle, determining when at least one other processor of said plurality of processors is not idle (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45)

a timer associated with each processor for timing from the beginning of receiving a process from the processor's queue, the duration of the time the process is run, during which time the processor is running the process is non-idle.(col. 2 lines 8-55, col. 6 lines 4-7,)

and poaching a process on a queue of the at least one non-idle processor to be run by said at least one processor which is idle (col. 11 lines 4-7, col. 14 lines 37-45)

timing a predetermined period of time during which said at least one other processor which is not idle remains not idle and poaching a process when the predetermined period of time has elapsed (col. 14 lines 37-45).

23. Kimmel does not specifically each processor having a cache associated therewith. It would have been obvious to one skilled in the art to have included a cache for each processor in Kimmel's system. By having a cache at each processor the access to memory will increase therefor increasing the throughput of the entire system.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nilesh R Shah whose telephone number is 703-305-8105. The examiner can normally be reached on Monday-Friday 8am-4pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on 703-305-9678. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

NS

January 7, 2004

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